Abstract

A memory buffer for a memory module board which is connected via a signal line (10-i) to a plurality of memory modules (2-i) mounted on said memory module board having different signal line lengths, wherein the memory buffer (1) comprises for each signal line (10-i) a corresponding integration circuit (18-i) for integrating the transmission time of a measurement pulse transmitted via said signal line (10-i) between said memory buffer (1) and a memory module (2-i) connected to said signal line (10-i).

(Figure 3)